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A Proposed H-Bridge Based Cascaded Multilevel Inverter for Speed Control of Induction Motor

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ABSTRACT:This paper introduces a novel H-bridge based cascaded multilevel inverter with reduced DC sources and switches. This topology introduces a low complexity thereby reducing the overall cost of an inverter. The proposed power circuit was used as a Proportional Integral controller whose switches are controlled by Phase Disposition pulse width modulation technique to control the speed of an induction motor. The simulation was carried out using Matlab / Simulink. The simulation of the same was made and performance of various PWM techniques such as Phase opposite disposition and phase shifted were compared on different quantitative measures such as Voltage, current stator Total harmonic Distortion, Voltage stress and settling time. It was observed that that the proposed power circuit with Phase disposition pulse width modulation that offers reduced total harmonic Detection in terms of voltage, current and phase was found to be very less when compared to other Pulse width modulation techniques. The controller still have a fast settling time thereby making this inverter a choice for real time speed control of induction motor.

KEYWORDS: Speed control, Phase disposition PWM, H bridge based cascaded Multilevel inverter, Inverter

I. INTRODUCTION

Competence of multilevel inverters (MLI) on lower voltage and larger power process that has reduced switching loss, lowered electromagnetic interference, increased quality of the power with reduced harmonics at lower level [1]. DC sources act as an input on set of power semiconductor device connected in an arrangement gives rise to stepped voltage waveform [2]. The MLI has three basic topologies. They are Diode clamped Multilevel Inverter (DCMLI), flying capacitor multilevel inverter (FCMLI), Cascaded Multilevel Inverter (CMLI) [3]. CMLI consists of either symmetric or Unsymmetrical H bridges based on the DC voltage sources. In symmetric type the magnitude of dc voltages of all H bridges are same and for the Unsymmetrical type the voltages differ in H Bridge [4]. Over the years various PWM techniques were used for multi-level inverters. The renowned PWM methods used for multi-level inverters are the carrier based PWM (SPWM) techniques and the space vector based PWM (SVPWM) techniques. The SPWM schemes are easy to implement and more flexible. These SPWM techniques use a triangular carrier waveform as carrier and sinusoidal signal as reference signal. Multilevel sinusoidal PWM are further classified into carrier and modulating signals. Based on the carrier signals the technique is further classified into Phase disposition (PD), Phase Opposition Disposition (POD), Phase shifted (PS) control technique, super imposed carrier, alternate POD and Hybrid technique. The various PWM techniques are used on the MLI to achieve desired output with reduced Total harmonic Distortion (THD), voltage stress across switches. An induction motor being rugged, reliable, and relatively inexpensive makes it more preferable in most of the industrial drives. They are mainly used for constant speed applications because of unavailability of the variable-frequency supply voltage [5]. In this work to increase the output voltage with reduced number of switches is proposed. A novel system for speed control of induction motor is introduced. A closed loop controller that acts as a PI controller will furnish the required PWM to control the speed of the induction motor. Different PWM techniques such as PD, POD, PS were employed on the power circuit and the performance of the system was evaluated using voltage THD, current THD, Stator THD, voltage stress and settling time of the controller. Section II gives the working of the three phase seven level cascaded H bridge multilevel inverter. Section III & IV gives the Modes of Operations, Section V to VIII gives the PWM Techniques used for three phase seven level cascaded H bridge multilevel inverter. Section IX gives the simulation and discussions of the power circuit fed on induction motor with different PWM techniques. Section X gives the conclusion of the paper.

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II. CASCADED MULTILEVEL INVERTER WITH H-BRIDGE

A Novel H Bridge based cascaded multilevel inverter is proposed. The power circuit will require less number of DC sources and switches. The topology consists of lower blocking voltage on switches, which results in decreased complexity and total cost reduction of the inverter. The Single Phase Seven Level Z –Source Cascaded H-Bridge Multilevel Inverter for seven level inverter is shown in Figure 1. The Power circuit consists of six unidirectional power switches (Sa1… Sa12) and DC Voltages Vdca1 & Vdca2. The switches Sa1… Sa4 (or Sa5… Sa8) simultaneously turn-on, which causes the voltage sources to short circuit. Therefore, the simultaneous turn-on of the mentioned switches to be avoided. In addition, Sa9 & Sa10 should be not be turn on at the same time. Table1 shows the output voltages of the proposed inverters for different states of the switches. In this table, 1 and 0 indicate the ON and OFF states of the switches, respectively Therefore the values of dc voltage sources should be different to generate more voltage levels without increasing the number of switches and dc voltages sources. The magnitude of Vdca1 and Vdc a2 should be considered 3 times and 1 time respectively. Similarly, for the topology shown in Figure 1, the magnitude of Vdca1 and Vdca2 should be considered 2 times and 1 times respectively. Considering the above details the total cost of the of proposed topology is low as compared to other topology, because of the dc voltage sources with low magnitude are needed. The three phase seen level Z source cascaded H Bridge Multilevel Inverter is shown in Figure 2. Proposed architecture differs from other circuits in the following ways. It has got the initial solution for the conflicts caused by Modulation Index and D, for the high power quality and high boost invention ability. The switching pattern for Proposed New Cascaded seven level inverter H-Bridge is shown in Table 1. In this, New Proposed New Cascaded Seven level Inverter Topology, the magnitude of the dc voltage sources of the seven level inverter is shown in Fig 1 are determines as follows:

$$\textbf{Vdc a1} = \textbf{Vdc} \quad \textbf{(1)}$$

$$\textbf{Vdc a2} = \textbf{3 Vdc} \quad \textbf{(2)}$$

Considering the above equations and parameters in the Table 1, the proposed new cascaded seven level inverter can generate 0 +/- Vdc, and 3 Vdc at output. The following are different PWM techniques used in simulating the proposed hardware circuit.

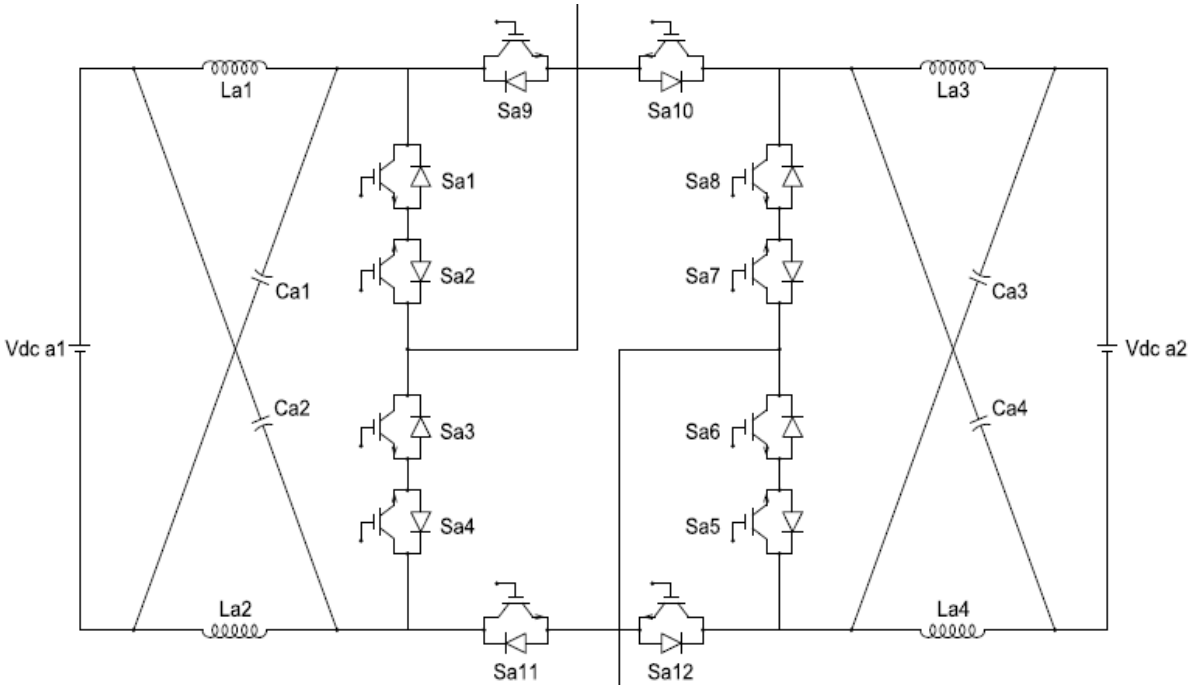

Figure 1 Single Phase Seven Level Z –Source Cascaded H-Bridge Multilevel Inverter

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Table 1 Proposed New Cascaded seven level inverter H-Bridge

S No	Sa1, Sa2	Sa3, Sa4	Sa5, Sa6	Sa7, Sa8	Sa9,Sa10	Sa11, Sa12	Vo
1	1	0	0	1	0	1	Vdca1
2	1	0	0	1	1	0	-Vdca2
3	1	0	1	0	0	1	Vdca1+Vdca2
4	1	0	1	0	1	0	0
	0	1	0	1	0	1	
5	0	1	1	0	1	0	-Vdca1
6	0	1	1	0	0	1	-Vdca2
7	0	1	0	1	1	0	-(Vdca2+Vdca1)

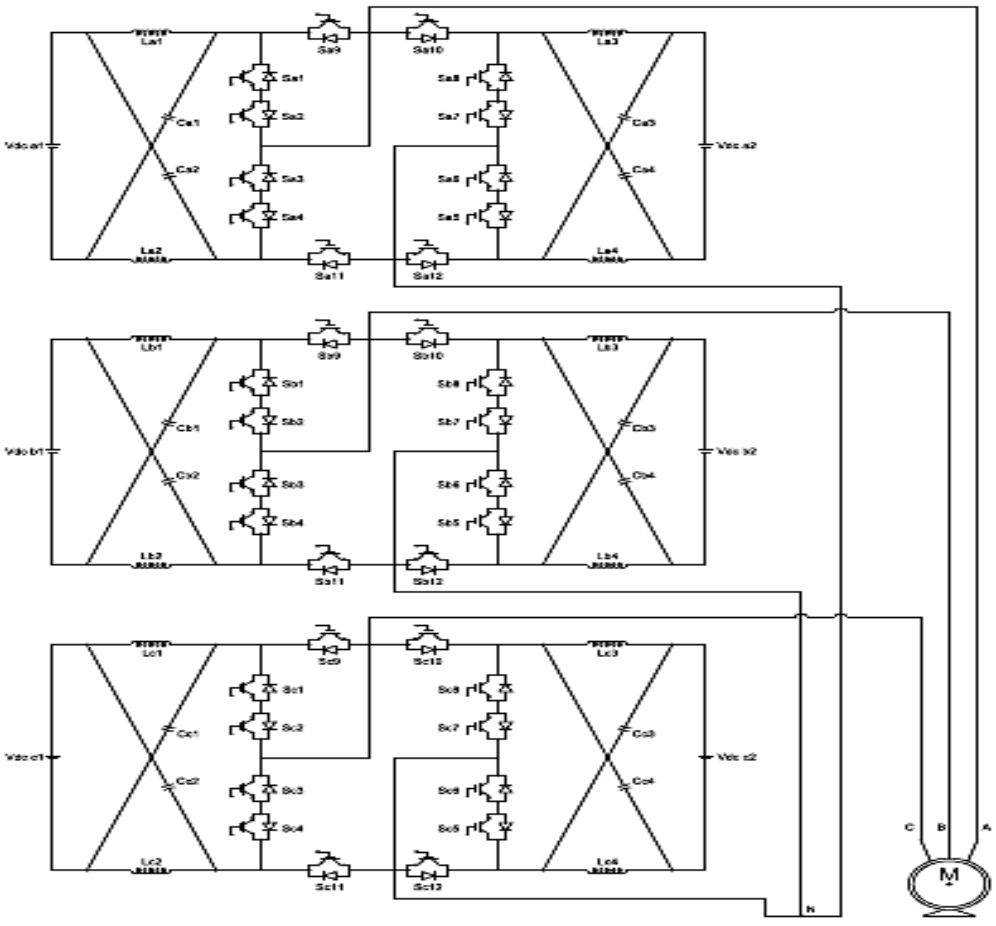

Figure 2 Proposed New Cascaded seven level inverter H-Bridge

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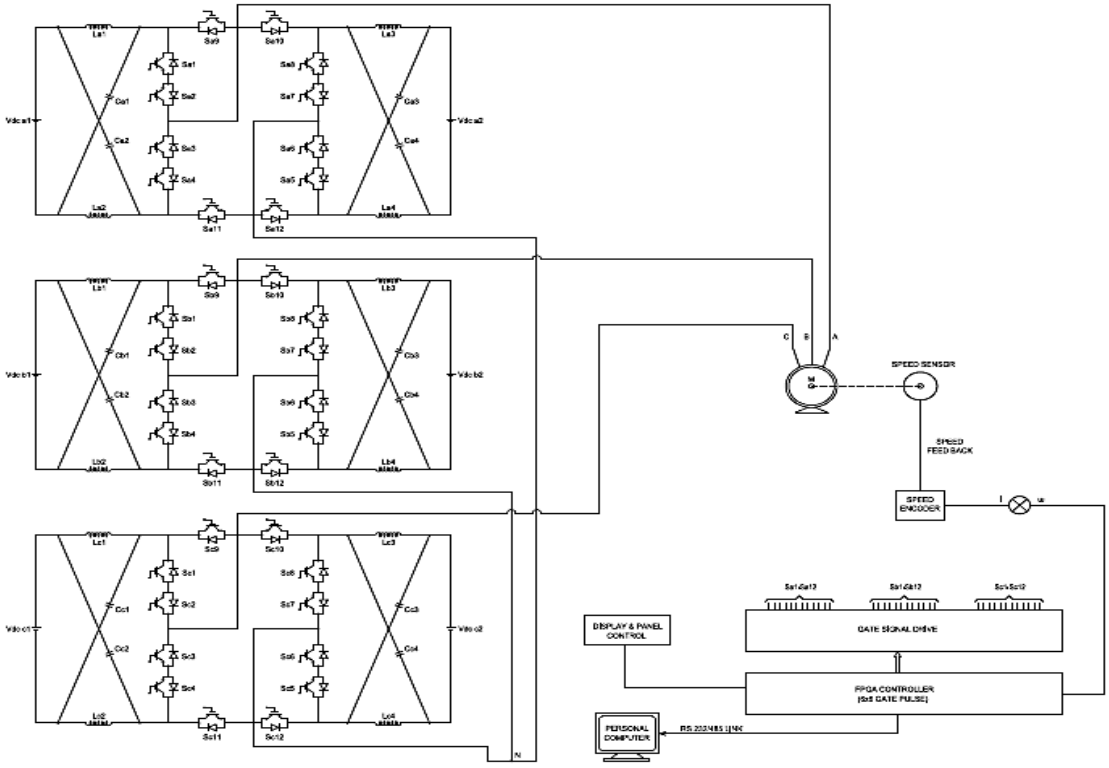

Figure 3 Closed loop Circuit Diagram Seven level Cascaded H Bridge Inverter

III. MODE -1 Non shoot through mode

The equivalent circuit during non-shoot through mode is shown in Figure 4. An inverter is in a non-shoot through state that is one of the six active states and two traditional open zero states and inductor current meets the following inequality:

$$\mathbf{i_L > 0.5\ I_i} \quad (3)$$

In this mode, the input DC current is

$$\mathbf{I_{in} = I_{L1}+I_{C1} = I_{L1}+(\ I_{L1}-i_1\ ) = \ 2i_L - i_1 > 0} \quad (4)$$

Voltage across the inductor is

$$\mathbf{V_L = V_0 - V_C} \quad (5)$$

Where $\mathbf{V_0}$ is the source voltage and Inductor current linearly decreases.

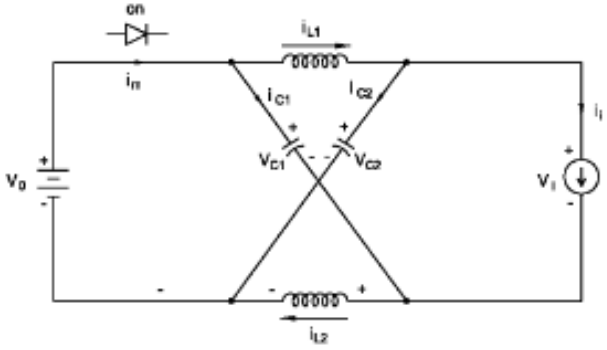

Figure4 Non Shoot through Mode equivalent circuit

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IV. MODE 2- SHOOT THROUGH MODE

The equivalent circuit in shoot through mode is shown in Figure 5. A switch shoot-through zero state occurs when the switches in any of the three phase legs are gated simultaneously

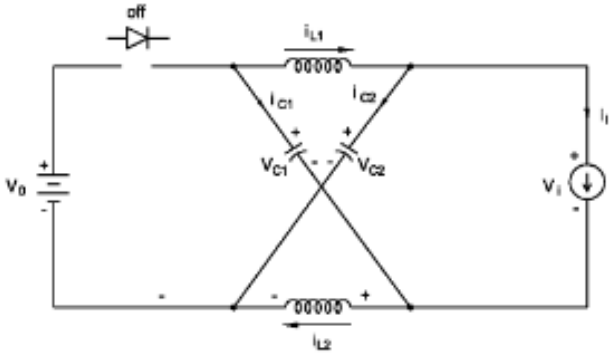

Figure 5 Shoot through mode equivalent circuit

This mode produces a zero voltage vector at the inverter output like open mode and contributes to the total active length of zero voltage state.
In this mode

$$\mathbf{V_{C1} + V_{C2} > V_0} \quad (6)$$

The diode is reverse biased, and the capacitors charge the inductors.
The Voltages across the inductors are:

$$\mathbf{V_{L1} = V_{C1}} \text{ and } \mathbf{V_{L2} = V_{C2}} \quad (7)$$

The inductor current linearly increases.

V. PWM TECHNIQUES

Over the years various PWM techniques were used for multi-level inverters. The renowned PWM methods used for multi-level inverters are the carrier based PWM (SPWM) techniques and the space vector based PWM (SVM) techniques. The SPWM schemes are easy to implement and more flexible. These SPWM techniques use a triangular carrier waveform as carrier and sinusoidal signal as reference signal. Multilevel sinusoidal PWM are further classified into carrier and modulating signals. Based on the carrier signals the technique is further classified into Phase disposition (PD), Phase Opposition Disposition (POD), Phase shifted (PS) control technique, super imposed carrier, alternate POD and Hybrid technique [7].

VI. PHASE DISPOSITION PWM TECHNIQUE (PD)

In this method all the carriers have the same frequency and amplitude. Also, the N-1 carriers are in phase with each other. This method uses N – 1 carrier signals to generate N level inverter output voltage. All the carrier signals have the same amplitude, same frequency carrier signals have the same amplitude, same frequency and are in phase [6]. Fourteen triangular carrier wave forms are compared with one sine wave. Figure 6 Illustrates the Phase Disposition Carrier Control Technique.

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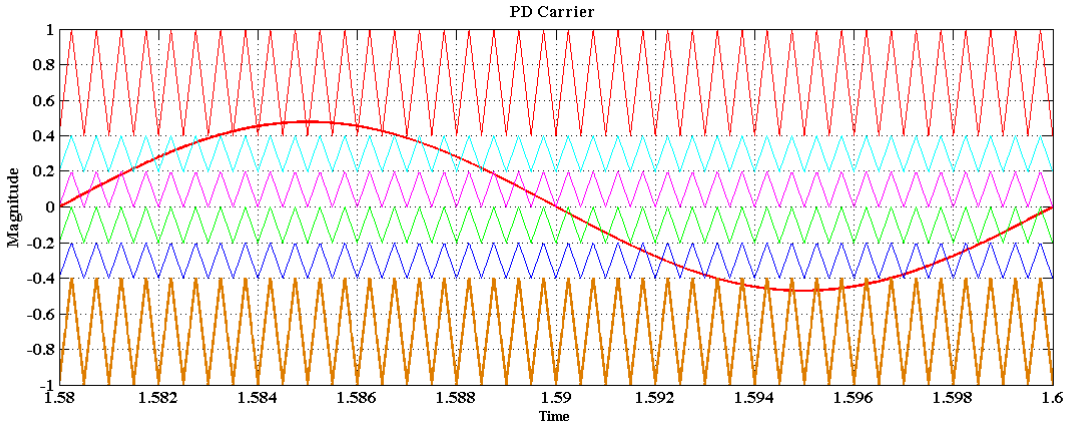

Figure 6 Phase Disposition (PD) Carrier Control Technique

VII. PHASE OPPOSITE DISPOSITION PWM (POD)

In this technique, the carrier signals about the zero reference has same frequency, amplitude and in phase to each other [6]. But below the zero axis the carrier signals are phase shifted by 180 degrees. It requires m-1 triangular carrier signals and the reference is sinusoidal in nature. The important harmonics is centered at Fc and other frequencies appear as side bands around Fc. Figure 7 Illustrates the Phase Opposite Disposition Carrier Control Technique.

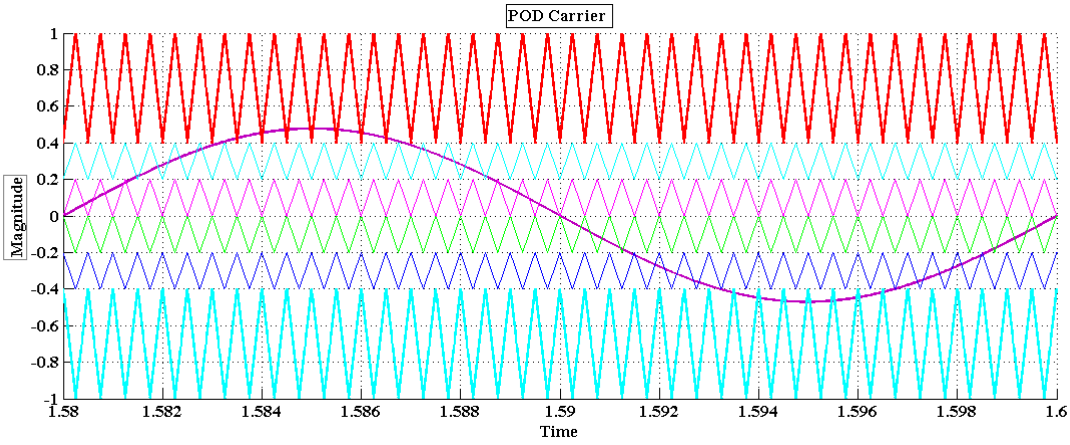

Figure 7 Phase Opposite Disposition (POD) Carrier Control Technique

VIII. PHASE SHIFTED CARRIER CONTROL TECHNIQUE: (PS)

In this technique the carrier signals are 90 degrees phase shifted to each other. All the triangular carrier have the same frequency and peak to peak amplitude. For a m voltage level required, m-1 carrier signals are required and they are shifted in phase by an angle $\theta = (360°/m-1)$ [7]. Figure 8 Illustrates the Phase Shifted Carrier Control Technique.

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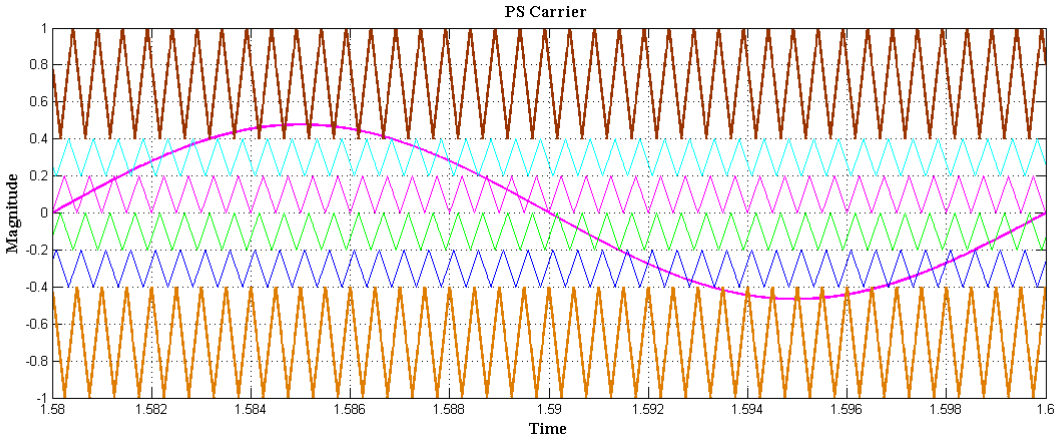

Figure 8 Phase Shifted (PS) Carrier Control Technique

IX. SIMULATIONS AND DISCUSSIONS

The proposed power circuit is connected to induction motor with speed of the induction motor is acquired using a speed sensor. The output of the sensor is given to a PI controller that produces desired PWM using the various PWM techniques such as PD, POD, PS. The quantitative parameters such as phase voltage THD, line voltage THD, Stator current THD, settling time and Stress across switches were compared based on the PWM technique applied to the power circuit. The entire simulation was done in MATLAB/SIMULINK and the results are shown below. MATLAB 2014b version was used for all the simulation.

The parameters used for the power simulation on various PWM techniques for seven level cascaded H bridge multilevel inverter. The two different DC link voltage applied to the power circuit are 75 V DC and 225 V DC respectively. The inverter power rating is 200watts with the inverter output voltage is 0-200 V AS RMS (Line to Line) with the switching frequency of 2Khz. The number of carrier used is three.

Figure 9 gives the Mat lab Simulation for Closed loop Circuit Diagram Proposed New Cascaded H Bridge Inverter Figure 10 illustrates the Stator Current and Torque Curve in Phase Disposition Carrier PWM Technique. Figure 11 briefs the Line to Line Voltage for Phase Disposition Carrier PWM Technique. Figure 12 gives the Phase Voltage for Phase Disposition Carrier PWM Technique. Figure 13 illustrates stator current THD, Line Voltage THD, Phase voltage THD in phase Disposition carrier PWM Technique. Figure 14 illustrates Reference Set Speed and Actual Speed Curve for Phase Disposition Carrier PWM Technique. Comparison of different measures on various PWM techniques on the proposed seven level cascaded H-bridge based multilevel inverter is given in Table 2. The proposed hardware with different PWM technique were employed and connected to an induction motor. Speed control of the induction motor is performed. From the exhaustive results tabulated the following were inferred. Various PWM techniques were applied on the power circuit and THD, stress and speed settling time were tabulated. From Table 2, it is clear that the proposed power circuit with Phase disposition PWM exhibits lower phase voltage THD, Line voltage THD, Stator current THD and voltage stress with a faster settling time. The PD based power circuit has a phase voltage THD of 26.58%, line voltage of 16.91%, stator current THD of 1.48%, voltage stress of 75V and 225V with a very high speed settling time of 0.075sec.

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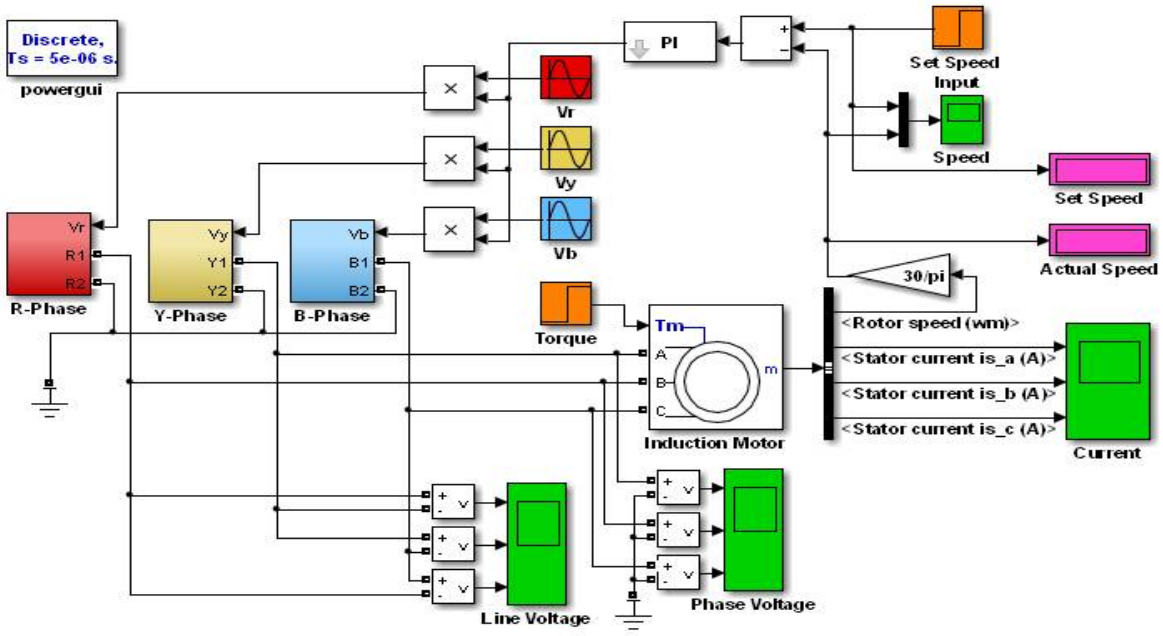

Figure 9Mat lab Simulation for Closed loop Circuit Diagram Proposed New Cascaded H Bridge Inverter

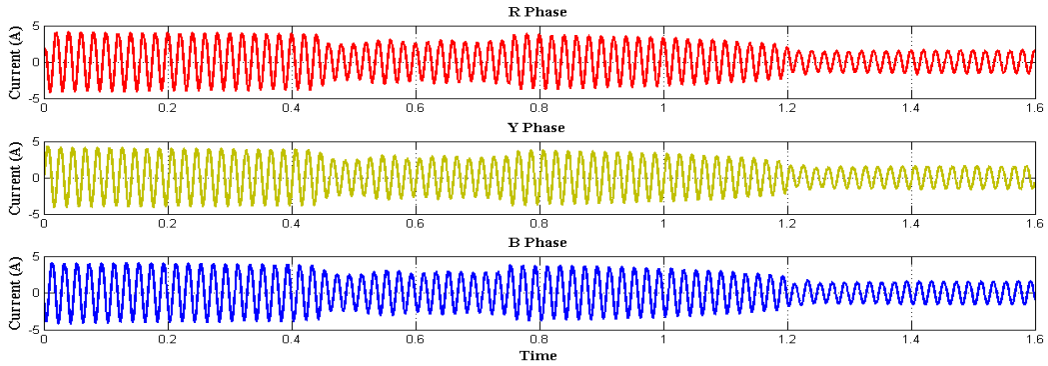

Figure 10 Stator Current and Torque Curve in Phase Disposition Carrier PWM Technique

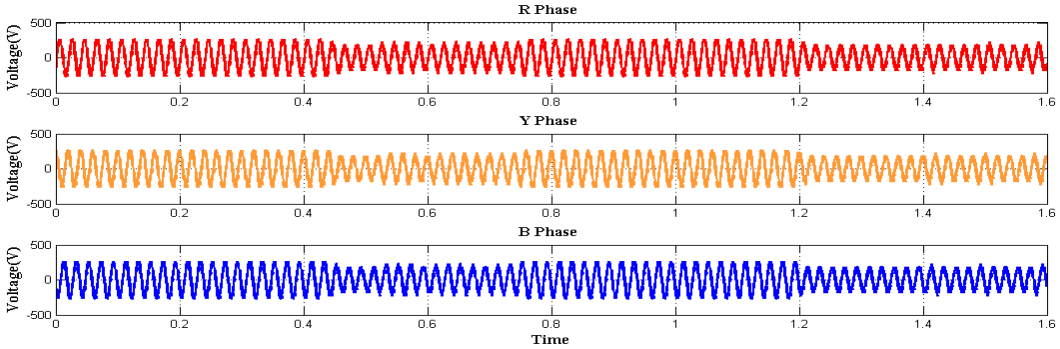

Figure 11 Line to Line Voltage for Phase Disposition Carrier PWM Technique

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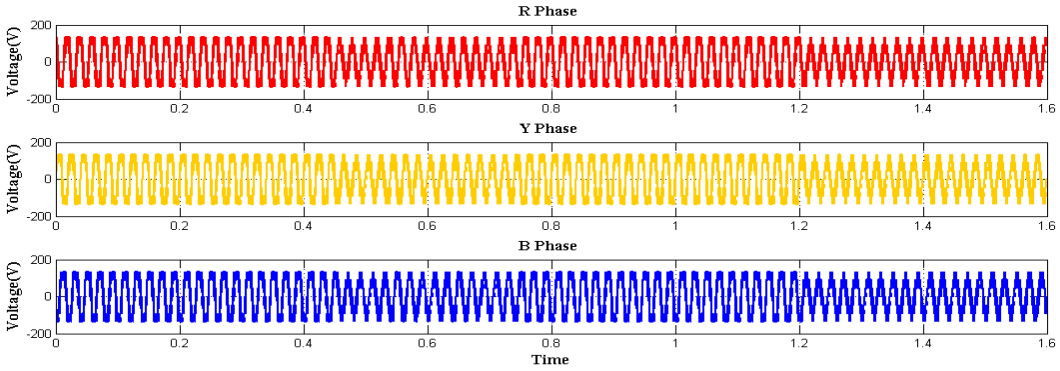

Figure 12 Phase Voltage for Phase Disposition Carrier PWM Technique

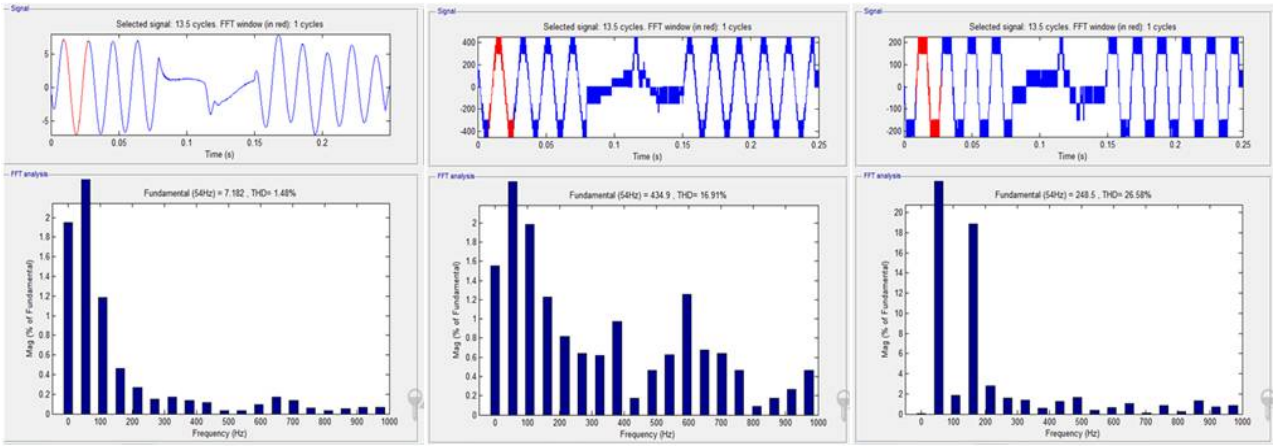

Figure 13 (a) stator current THD (b) Line Voltage THD (c) Phase voltage THD in phase Disposition carrier PWM Technique

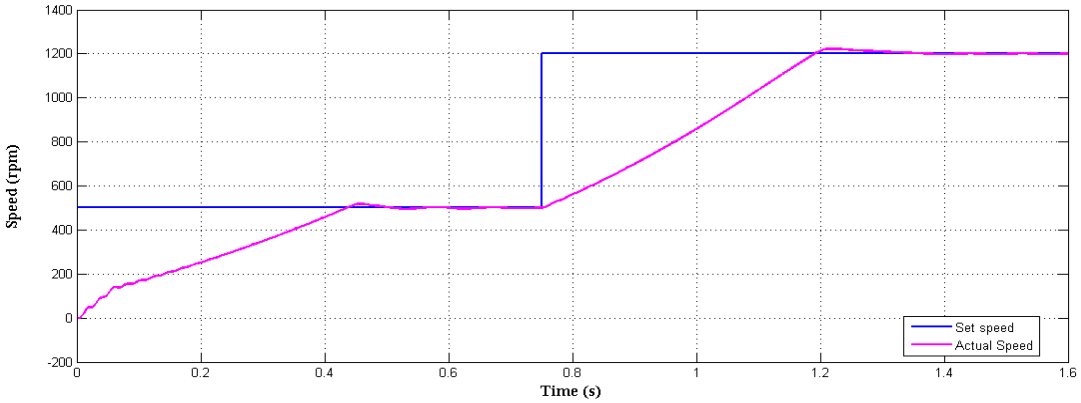

Figure 14 Reference Speed and Actual Speed Curve for Phase Disposition Carrier PWM Technique

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Table 2: Comparison of different measures on various PWM techniques on seven level cascaded multilevel inverter

PWM Technique	Phase Voltage THD	Line Voltage THD	Stator Current THD	Voltage Stress	Speed settling time
PD	26.58%	16.91%	1.48%	75V & 225V	0.075Sec
POD	33.39%	26.33%	4.88%	75V & 225V	0.13Sec
PS	39.8%	52.3%	6.59%	75V & 225V	0.28 Sec

X. CONCLUSION

The paper gives a novel power circuit with phase disposition PWM used for controlling. The combination provides a lower total harmonic distortion in terms of phase voltage, line voltage and stator current. The controller settles very quickly with the setting time of 0.075sec. Hence the above combination provides excellent result for the speed control of induction motor.

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